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Field-Effect Transistors from Lithographically Patterned Cadmium Selenide Nanowire Arrays

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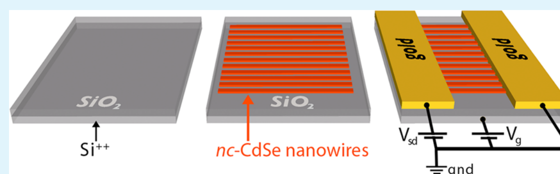

ABSTRACT: Field-effect transistors (NWFETs) have been prepared from arrays of polycrystalline cadmium selenide (pc-CdSe) nanowires using a back gate configuration. pc-CdSe nanowires were fabricated using the lithographically patterned nanowire electrodeposition (LPNE) process on SiO_2/Si substrates. After electrodeposition, pc-CdSe nanowires were thermally annealed at 300 °C × 4 h either with or without exposure to $CdCl_2$ in methanol—a grain growth promoter. The influence of $CdCl_2$ treatment was to increase the mean grain diameter from 10 to 80 nm as determined by grazing incidence X-ray diffraction and to convert the crystal structure from cubic to wurtzite. Measured transfer characteristics showed an increase of the field effect mobility (μ_{eff}) by an order of magnitude from 1.94×10^{-4} cm^2/(V s) to 23.4×10^{-4} cm^2/(V s) for pc-CdSe nanowires subjected to the $CdCl_2$ treatment. The $CdCl_2$ treatment also reduced the threshold voltage (from 20 to 5 V) and the subthreshold slope (by ~35%). Transfer characteristics for pc-CdSe NWFETs were also influenced by the channel length, L. For $CdCl_2$-treated nanowires, μ_{eff} was reduced by a factor of eight as L increased from 5 to 25 μm. These channel length effects are attributed to the presence of defects including breaks and constrictions within individual pc-CdSe nanowires.

KEYWORDS: *NWFET, mobility, lithography, electrodeposition, annealing, channel length*

INTRODUCTION

Field-effect transistors based upon semiconductor nanowires (NWFETs) were first prepared from semiconducting carbon nanotubes by Avouris[1] and Dekker[2] and coworkers in 1998. In 2000, Lieber and coworkers[3] prepared the first NWFETs from single crystalline silicon nanowires. Soon thereafter, a comparison of silicon NWFET transport metrics with their thin film counterparts[4] showed that the performance of NWFETs could substantially exceed that of thin film transistors (TFTs). This is one reason that the semiconductor industry is actively pursuing NWFET technology.[5]

Cadmium selenide (CdSe) is an n-type semiconductor (E_g = 1.70 eV) that has moderately high electron mobilities of μ_{eff} = 650−800 cm^2/(V s) at 298 K.[6,7] CdSe is of interest because of its utility in photonic devices such as photodetectors,[8−12] light emitting diodes,[13] and solar cells.[14−17] FETs based upon polycrystalline CdSe thin films[18−21] and NWFETs based upon single crystalline CdSe nanowires[22−27] have both been studied (Table 1). Electron mobilities in thin film CdSe transistors (TFTs) have ranged from 0.02 cm^2/(V s)[21] to 15 cm^2/(V s),[19] and CdSe NWFETs have produced comparable electron mobilities on average, but across a wider range from 5×10^{-4} cm^2/(V s)[23] to 800 cm^2/(V s).[27] The latter value,[27] which equals the bulk electron mobility in CdSe, is especially remarkable since it is nearly a factor of 100 higher than the electron mobilities measured in any other investigation of CdSe NWFETs (Table 1).

All of the CdSe NWFETs reported until now have been prepared from single crystalline nanowires synthesized using ″bottom-up″ methods, such as vapor−liquid−solid (VLS) growth.[28,29,3,30] For these nanowires, fabrication of a NWFET requires the isolation of a single nanowire, or ensembles of oriented nanowires, starting from a powder of orientationally disordered nanowires. This tedious process involves the spin coating of nanowires at low coverage onto a substrate followed by the application of metal contacts to each nanowire using electron beam lithography (EBL).[3] In the case of nanowire arrays, additional processing steps are required to impart some degree of alignment to ensembles of nanowires. This can be accomplished, for example, by preparing source and drain electrodes and using dielectrophoresis to migrate nanowires in solution into the channel between these two electrodes.[31−34] NWFETs have also been achieved using ″top-down″ processing starting with CMOS-compatible silicon-on-insulator (SOI) wafers, isolating a nanowire using a combination of EBL and etching, and finally applying a top gate to the nanowire.[35−37] Top-down processing has the advantage that the orientation and doping of the nanowire can be precisely controlled, but slow EBL is still required to produce nanowires with widths in the sub 200 nm range from SOI wafers.

In this paper, we describe the preparation of NWFETs prepared from arrays of polycrystalline CdSe (pc-CdSe) nanowires. With the exception of silicon,[38−40] NWFETs have not been prepared from pc nanowires or nanowire arrays until now. These pc-CdSe nanowires were synthesized using the lithographically patterned nanowire electrodeposition (LPNE)

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Table 1. Comparison of Device Metrics for CdSe Thin Film and Nanowire FETs

description[a]	L (× W)[b] (μm)	μ_{eff} (cm^2/(V s))	V_{th} (V)	S (mV/dec)	ref
pc thin film CdSe tf	8 (× 293)	1	6.7	7000−10000	18
pc thin film CdSe tf	100 (× 500)	1−6.7	2.5−30	260−5000	20
pc thin film CdSe tf	20 (× 200)	15	3.5	500	19
nc thin film CdSe tf	100−200 (× 1−2 mm)	0.02−0.6		60	21
sc CdSe nr	3.2	9.6	20.9		25
sc CdSe nw	1	0.5			22
sc CdSe nw	18.3	0.77			26
sc CdSe nw	2	5×10^{-4}			23
sc In-doped CdSe nw	2	0.1−6.7			23
sc Cd-doped CdSe nr	20	800	-4.1	65	27
sc In-doped CdSe nw	5	3.2−166	−1.7−(−40)	$508-10^6$	24
pc CdSe nw:[c]					
annealed only[d]	5	1.9 (±0.2) × 10^{-4}	18−25	3600	this work
$CdCl_2$ treated & annealed[e]	5	23 (±5) × 10^{-4}	4−8	2300	this work

[a]Abbreviations: pc = polycrystalline, tf = thin film, sc = single crystalline, nw = nanowire, nr = nanorod. [b]Channel length, L, and width, W. All samples undoped unless otherwise specified. [c]NWFETs contained 100 (± 5) pc-CdSe nanowires. [d]Samples were thermally annealed at 300 °C for 4 h in N_2. [e]Samples were treated by immersing for 10 s in saturated $CdCl_2$ in methanol and then thermally annealing at 300 °C for 4 h in N_2.

method[41−43] which provides a means for patterning pc-CdSe nanowires across wafer-scale regions of a surface.[11,12] We compare pc-CdSe nanowires that were subjected to either of two post-processing treatments. All samples were thermally annealed at 300 °C × 4 h in nitrogen, but some nanowires were first exposed to $CdCl_2$ in methanol. $CdCl_2$ is a grain growth promoter for cadmium chalcogenides[44,45,14] and a chlorine dopant source.[46] We compare the properties of $CdCl_2$-treated and untreated pc-CdSe nanowires and the performance of arrays of $CdCl_2$-treated and untreated pc-CdSe nanowires in NWFETs.

EXPERIMENTAL SECTION

Nanowire Fabrication. The preparation of pc-CdSe nanowires on glass surfaces using the LPNE method has been described in detail previously.[12,11] In the first step of the LPNE process, a nickel layer is thermally evaporated onto RCA-cleaned, oxidized silicon substrates, SiO_2 (300 nm)/Si(p^+). Then a (+)-photoresist (PR) layer (Shipley 1808) is spin-coated, photopatterned, and developed, and the exposed nickel is removed by nitric acid etching. The etching duration is adjusted to produce an undercut around 300 nm in width at the edges of the exposed PR. This undercut produces a horizontal trench with a precisely defined height equal to the thickness of the Ni layer. Within this trench, pc-CdSe nanowires were electrodeposited using the scanning electrodeposition/stripping method, also as previously described.[12,11,47−49] The aqueous plating solution was unstirred aqueous 0.30 M $CdSO_4$, 0.70 mM SeO_2, and 0.25 M H_2SO_4 at pH 1−2. In addition to the LPNE-patterned nickel electrode, a saturated calomel reference electrode (SCE) and a 2 cm^2 platinum foil counter electrode were also employed in conjunction with a one-compartment three-electrode electrochemical cell and a Gamry G300 potentiostat. pc-CdSe was deposited by scanning the potential of the lithographically patterned Ni edge from −0.4 to −0.8 V vs SCE at 50 mV/s. On the initial negative scan from −0.4 to −0.8 V, CdSe was electrodeposited on the nickel electrode together with excess elemental cadmium. On the subsequent positive-going scan, excess elemental cadmium was oxidatively stripped from the nascent nanowire leaving stoichiometric CdSe (Figure 1b). A total of three scans were used to prepare the 60 nm (h) × ~150 nm (w) pc-CdSe nanowires incorporated into transistors in this study. After the electrodeposition process was complete, the lithographically patterned nickel electrode and the associated PR were both removed using nitric acid and acetone, respectively. Arrays of 100 linear pc-CdSe nanowires were patterned at 5 μm pitch onto the SiO_2/Si substrate (Figure 1e,f). pc-CdSe nanowires were treated using either of two post-deposition processes:[12,11] (1) thermal annealing at 300°C for 4 h in N_2 or (2) exposure to saturated $CdCl_2$ in methanol solution[12,11,50,14,51] for 10 s, followed by thermal annealing at 300 °C for 4 h in N_2. After thermal annealing, these pc-CdSe nanowires were rinsed with Milli-Q water to remove residual $CdCl_2$.

Device Fabrication. Lithographically patterned pc-CdSe nanowires were electrodeposited on highly doped p-type silicon substrates that were coated with 300 nm thermally grown gate oxide. Gold source and drain electrodes Au/Cr (50 nm/1 nm) were patterned onto both ends of the pc-CdSe nanowires by a photolithography and lift-off process (Figure 1d). The underlying conducting Si (resistivity: 0.001−0.004 Ω cm) was used as a back gate. Devices with three channel lengths, L, were evaluated: 5 (Figure 1e), 10, and 25 μm. Measurements were conducted in a common source configuration (Figure 1a, right).

pc-CdSe Characterization. Scanning electron microscopy (SEM) images were acquired using a Philips XL-30 FEG (field emission gun) SEM using an accelerating voltage of 10 keV. All samples were sputtered with a thin layer of Au/Pd prior to imaging to prevent charging. Grazing-incidence X-ray diffraction (GIXRD) patterns were obtained using a Rigaku Ultima III high-resolution X-ray diffractometer employing the parallel beam optics with a fixed incident angle of 0.30°. The X-ray generator was operated at 40 kV and 44 mA with Cu Kα

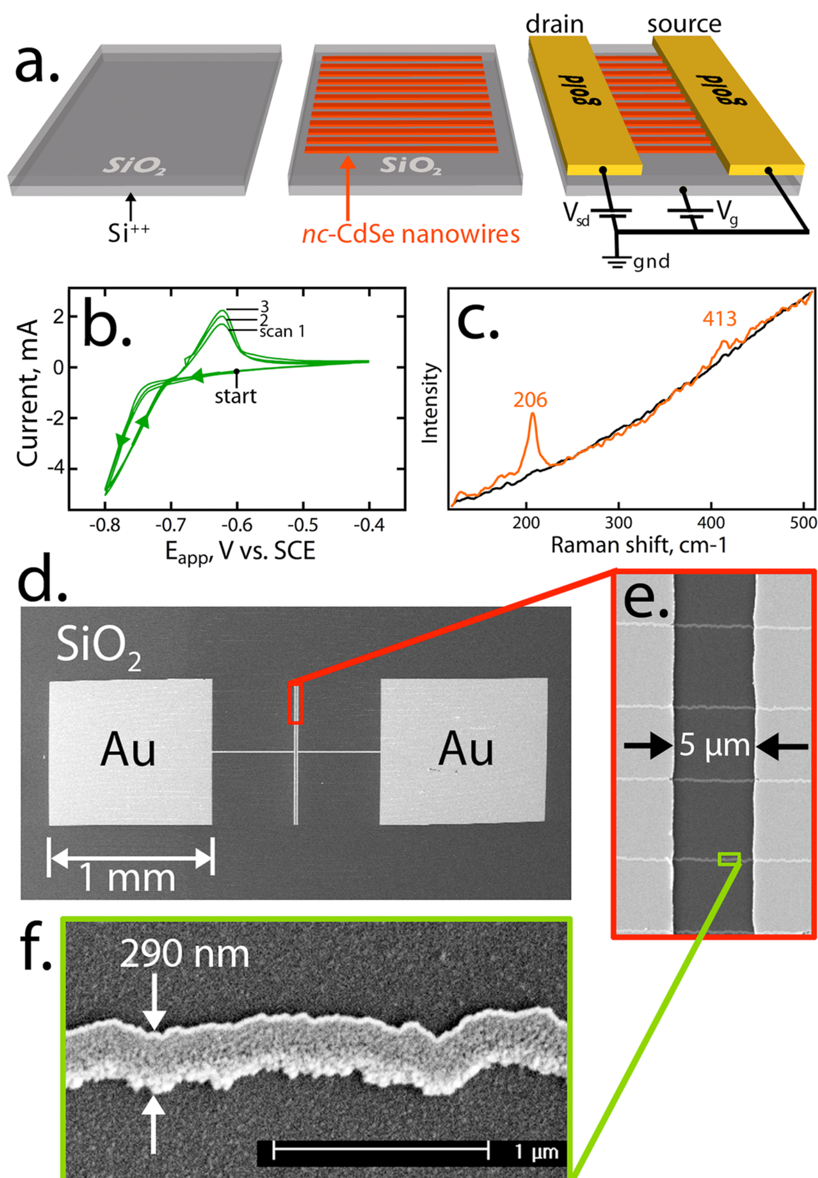

Figure 1. Fabrication of pc-CdSe NWFETs. (a) Schematic diagram depicting the three-step NWFET fabrication process starting with a SiO_2-covered p^+-silicon surface (left). An array of pc-CdSe nanowires is then prepared using LPNE (middle). Finally, gold source and drain electrodes are patterned by photolithography (right). (b) Current versus potential traces at 50 mV/s for the synthesis by scanning electrodeposition/stripping of pc-CdSe nanowires within the LPNE template electrode. The plating solution contains 0.30 M $CdSO_4$, 0.70 mM SeO_2, and 0.25 M H_2SO_4 at pH 1−2. (c) Raman scattering spectra (λ_{ex} = 532 nm) of a pc-CdSe nanowire array on glass (orange trace) and a clean glass surface (black trace). (d−f) Scanning electron microscopy (SEM) images of the electrical contacts and contact pads (d), the 5 μm channel showing five CdSe nanowires (horizontal) (e) and a single CdSe nanowire. The growth direction for this nanowire was from top to bottom (f).

irradiation. The JADE 7.0 X-ray pattern data processing software (Materials Data, Inc.) was used to analyze acquired patterns and estimate the respective grain diameter size. Raman spectra were collected using a Renishaw inVia Raman Microscope equipped with the Easy-Confocal optical system (spatial resolution less than 1 μm) using a 532 nm laser and a 2400 line/mm grating. An optical power of 50 mW was used in conjunction with an integration time of 30 s. WiRE 3 software was used to acquire the data and images. Atomic force microscopy (AFM) images were acquired using an Asylum Research, MFP-3D AFM equipped with Olympus, AC160TS tips in a laboratory air ambient.

NWFET Electrical Characterization. Electrical characteristics of pc-CdSe NWFETs were measured using a Keithley 2400 sourcemeter and a Keithley 428 current amplifier both controlled by LabVIEW software. The source-drain current, I_{sd}, was measured as a function of the source-drain voltage, V_{sd}, at gate voltages, V_g, ranging from −10 to 60 V. Values of the transconductance, g_m, and the threshold voltage, V_{th}, were determined from I_{sd} versus V_{gs} curves using the linear region of these curves[25,27]

$$g_m = \frac{dI_{sd}}{dV_{gs}} \quad (1)$$

For CdSe nanowires with a rectangular cross section, the gate capacitance per unit length can be calculated using eq 2[52]

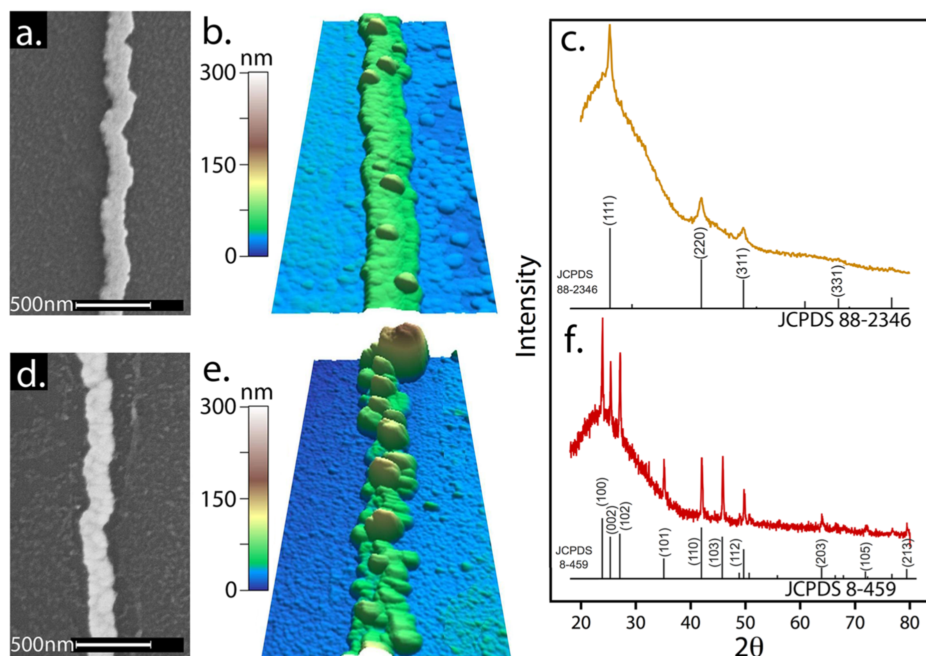

Figure 2. (a,d) SEM images and atomic force microscopy (AFM) images (b,e) of as-deposited pc-CdSe nanowires that were thermally annealed (300 °C, 4 h, N_2) (a,b) and pc-CdSe nanowires dipped in saturated $CdCl_2$, methanol solution (10 s), and thermally annealed (300 °C, 4 h, N_2) (d,e). (c,f) Grazing incidence X-ray diffraction (GIXRD) patterns of: (c) as-deposited pc-CdSe nanowires that were thermally annealed (300 °C,4 h, N_2), (f) dipped in saturated $CdCl_2$, methanol solution (10 s) and annealed (300 °C, 4 h, N_2).

$$C = \varepsilon_o \varepsilon_r \left[\frac{w - t/2}{h} + \frac{2\pi}{\ln(1 + 2h/t + \sqrt{2h/t(2h/t + 2)})} \right] \tag{2}$$

where w is the mean width of the nanowires; t is the mean height; and h is the gate oxide thickness (300 nm). Linear range carrier mobilities, μ_{eff}, were estimated according to eq 3.[22,23,27,53]

$$\mu_{eff} = \frac{g_m L^2}{NCV_{sd}} \tag{3}$$

where N is the number of nanowires. The electron carrier concentrations, n_e, were estimated from the equation[54,27]

$$n_e = \frac{CV_{th}}{ewtL} \tag{4}$$

Threshold voltage V_{th} was estimated from the linear region of the I_{sd} versus V_{gs} plot by extrapolation to the abscissa.[6,18,25] The subthreshold slope, S, was calculated from transfer curves in the interval $V_{th} < V_{gs} < (V_{th} + 4\ \text{V})$ according to[6]

$$S = \frac{dV_{gs}}{d(\log I_{sd})} \tag{5}$$

The on−off current ratio I_{on}/I_{off} was obtained from the logarithmic plot of I_{sd} versus V_{gs} where I_{on} is the current value at the threshold voltage and I_{off} is the current value when the device is in the off state.[25]

RESULTS AND DISCUSSION

Synthesis and Characterization of pc-CdSe Nanowires. Arrays of pc-CdSe nanowires prepared using LPNE were used as the starting point for the fabrication of NWFETs in this study (Figure 1a). As previously described,[11,12] stoichiometric pc-CdSe nanowires were obtained using the scanning electrodeposition/stripping method.[47] An aqueous plating solution containing 0.30 M $CdSO_4$, 0.70 mM SeO_2, and 0.25 M H_2SO_4 at pH 1−2[49,55] was used to electrodeposit both CdSe and elemental cadmium on an initial negative-going voltammetric scan from −0.60 to −0.80 V vs SCE. The electrodeposition of elemental selenium, although thermodynamically possible, does not occur because the Cd:Se ratio in this plating solution is 43:1. As the potential is scanned positively from −0.80 V (Figure 1b), excess elemental Cd is removed from the nascent pc-CdSe nanowires at −0.62 V to produce nanowires of near stoichiometric pc-CdSe. As-deposited pc-CdSe nanowires prepared by LPNE did not show a gate effect in spite of the fact that the electrical conductivity of these nanowires is just ∼20% higher than for CdSe nanowires that were thermally annealed at 300 °C × 4 h in nitrogen and which did demonstrate a gate effect (vide infra).[12] For this reason, all pc-CdSe nanowires examined in this study were subjected to thermal annealing, but some nanowires were exposed to saturated $CdCl_2$ in methanol before this thermal treatment. Exposure to $CdCl_2$ in methanol prior to thermal annealing has been shown to promote grain growth in CdSe,[44,45,14] and it has also been used as a chlorine dopant source.[46] Recently,[11,12] we found that $CdCl_2$ treatment increases both the mean grain diameter and the photoconductive gain for arrays of pc-CdSe nanowires configured as photodetectors.

Arrays of pc-CdSe nanowires were characterized using scanning electron microscopy (SEM), atomic force microscopy (AFM), X-ray diffraction (XRD), and Raman spectroscopy before the patterning of gold source and drain electrodes. Raman spectra acquired using λ_{ex} = 532 nm were identical for pc-CdSe nanowires that were treated with $CdCl_2$ (wurzite phase) and those that were not (zinc blende phase). In both cases, transitions at 206 and 413 cm^{-1}, assigned to the longitudinal optical (LO) phonon and to 2LO, respectively,

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Table 2. Performance Metrics for NWFETs Prepared Using Lithographically Patterned pc-CdSe Nanowire Arrays[a]

L (μm)	n_e[b] (cm^{-3})	μ_{eff}[c] (cm^2/(V s))	V_{th} (V)	S[d] (mV/dec)	C[e] (fF)	g_m[f] (nS)	I_{on}/I_{off}
thermally annealed[g]							
5	1.8 (±0.3) × 10^{18}	1.9 (±0.2) × 10^{-4}	18–25	3600	0.39	0.046	~80
10	3.6 (±0.1) × 10^{18}	6 (±2) × 10^{-5}	42–46	4800	0.78	0.02	~75
25	3.6 (±0.3) × 10^{18}	8 (±3) × 10^{-6}	50–60	7100	1.6	0.0005	~40
treated with CdCl$_2$/MeOH and thermally annealed[h]							
5	5 (±2) × 10^{17}	23 (±5) × 10^{-4}	4–8	2300	0.39	0.76	~320
10	10 (±2) × 10^{17}	9 (±5) × 10^{-4}	10–15	3300	0.78	0.06	~240
25	1.3 (±0.3) × 10^{18}	3 (±2) × 10^{-4}	17–25	4500	1.6	0.009	~210

[a]NWFETs contained 100 (± 5) pc-CdSe nanowires. [b]Electron concentration. [c]Linear range electron mobility. [d]Subthreshold slope, with units of voltage per decade current. [e]Capacitance. [f]Transconductance. [g]Samples were thermally annealed at 300 °C for 4 h in N$_2$. [h]Samples were treated by immersing for 10 s in saturated CdCl$_2$ in methanol and then thermally annealing at 300 °C for 4 h in N$_2$.

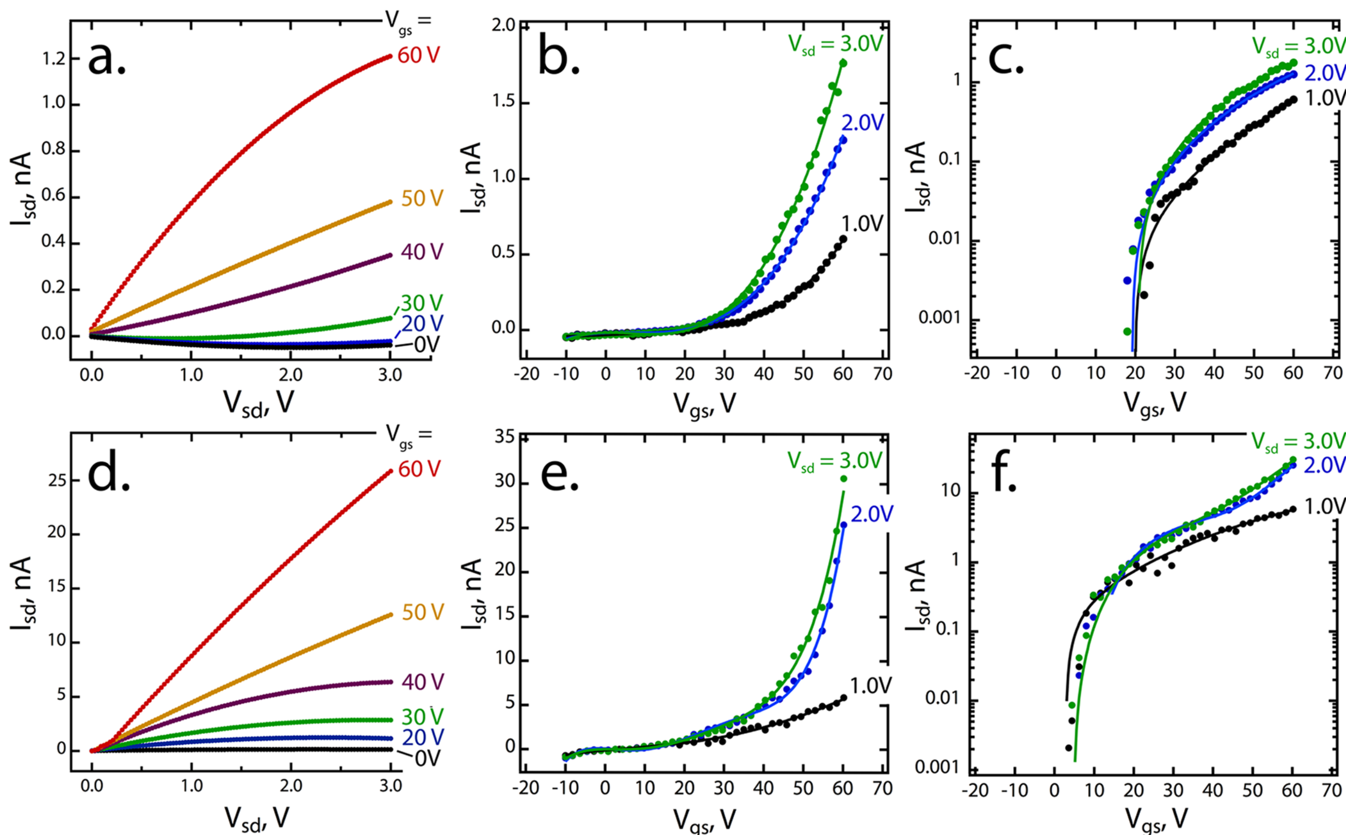

Figure 3. Electrical characterization of $L = 5$ μm NWFETs based on pc-CdSe nanowire arrays. Shown in (a,b,c) are data for nanowires that were not treated with CdCl$_2$ and in (d,e,f) are data for CdCl$_2$-treated nanowires: (a,d) I_{sd} versus V_{sd} traces as a function of V_{gs}. (b,e) I_{sd} versus V_{gs} transfer characteristics for three V_{sd} values and (c,f) log-linear plot of the same data shown in (b,e).

were observed (Figure 1c), in accordance with prior work on CdSe.[56,57] This spectrum is consistent with CdSe since the LO phonon energy for CdSe single crystals is 209 cm^{-1} whether these crystal structures are wurtzite or zinc blende.[58]

The influence of the CdCl$_2$ treatment is apparent in scanning electron microscope (SEM) and atomic force microscope (AFM) images of these pc-CdSe nanowires (Figure 2). Both SEM (Figure 2a,d) and AFM (Figure 2b,e) analysis show that CdCl$_2$ treatment causes roughening of the nanowire surface as a consequence of rapid grain growth. Especially clear in AFM images of CdCl$_2$-treated pc-CdSe nanowires are individual CdSe grains (Figure 2e). Grazing-incidence X-ray diffraction (GIXRD) analysis was performed on pc-CdSe nanowires, and the mean grain diameter, d_{ave}, was estimated from the X-ray line width using the Scherrer equation[59]

$$d_{ave} = 0.89\frac{\gamma}{B\cos\theta} \quad (6)$$

where γ is the X-ray wavelength; B is the full width of the peak measured at half-height; and θ is the diffraction angle. GIXRD patterns for pc-CdSe nanowires that were not treated with CdCl$_2$ (Figure 2c) show three reflections assignable to a zinc blende structure. Line broadening permits an estimate of d_{ave} = 10 nm. A completely different GIXRD pattern, assignable to wurtzite CdSe, is observed for CdCl$_2$-treated pc-CdSe nanowires. The narrower lines in this pattern correspond to d_{ave} = 80 nm. The influence of the CdCl$_2$ treatment on the grain

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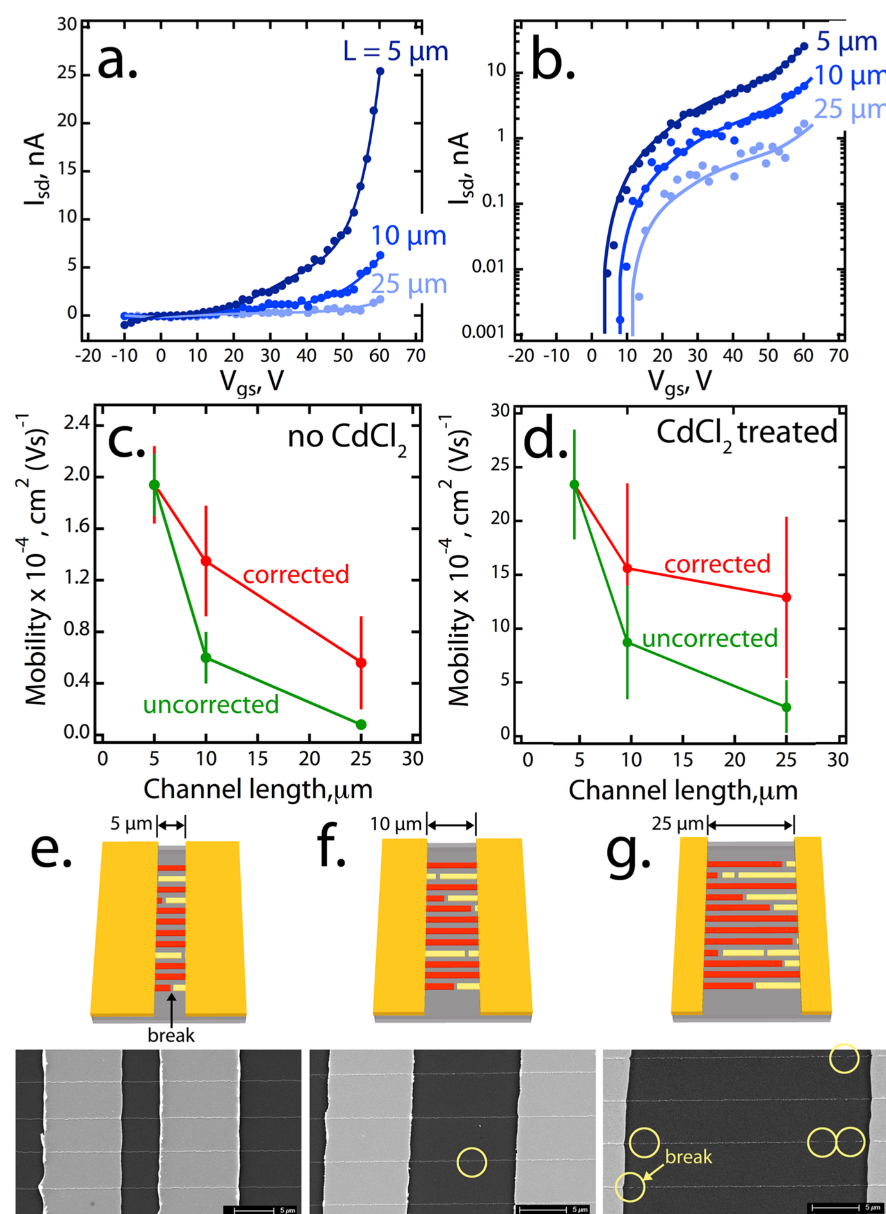

Figure 4. Influence of the channel length, L, on the transfer characteristics for $CdCl_2$-treated and annealed pc-CdSe NWFETs. (a) I_{sd} versus V_{gs} plots at V_{sd} = 2 V for three channel lengths as indicated. (b) log I_{sd} versus V_{gs} curves for three channel lengths as indicated. (c) Linear range carrier mobilities, μ_{eff}, versus channel length for pc-CdSe NWFETs not treated with $CdCl_2$ before (green trace) and after (red trace) correcting for discontinuous nanowires. (d) Same plot as (c) for pc-CdSe NWFETs that were $CdCl_2$ treated. (e−g) Schematic diagrams of NWFET devices (top) and SEM images (bottom) for L = 5 μm (d), L = 10 μm (e), and L = 25 μm (f) showing an increase in the number of discontinuities with increasing L.

diameter and the crystal structure are consistent with our previous results[11,12] as well as the previous works of others.[60−63]

The electrical properties of pc-CdSe NWFETs were examined for devices containing 100 (±5) nanowires having three different channel lengths: 5, 10, and 25 μm. Performance metrics for these devices are summarized in Table 2. In a common source configuration (Figure 1a, right), the application of positive V_{gs} strongly enhances I_{sd} versus V_{sd} both for $CdCl_2$-untreated (Figure 3a) and $CdCl_2$-treated (Figure 3d) pc-CdSe nanowires. These output characteristics are consistent with enhancement mode operation for an n-type channel,[6] just as previously reported for FETs prepared from polycrystalline CdSe films[18−21] and single crystalline CdSe nanowires.[25,22,26,23,27,24]

Transfer characteristics for the same two devices shown in Figure 3a,d show a threshold voltage of 18−25 V for $CdCl_2$-untreated (Figure 3b,c) nanowires and 4−8 V for $CdCl_2$-treated (Figure 3e,f) pc-CdSe nanowires. These voltage ranges reflect the device-to-device variability in V_{th} for 3−5 NWFETs at each channel length value. The threshold voltage for a CdSe NWFET has been reported in just one previous study to our knowledge: V_{th} = 20.9 V was observed by Lee and coworkers[25] for NWFETs (L = 3.2 μm) prepared from individual undoped single crystalline CdSe nanoribbons (width = 630 nm) synthesized by evaporation. Several studies involving thin film pc-CdSe FETs have achieved lower V_{th} values[18−20] ranging

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from 2.5[20] to 6.7 V[18] (Table 1). This performance pertains to devices prepared from undoped CdSe. With intentional doping by either cadmium[27] or indium,[24] V_{th} shifts sharply to voltages as negative as −40 V.[27]

The sensitivity of a FET to gate inputs just below V_{th} is measured by the subthreshold slope, S, defined as the change in the gate voltage necessary to induce a change in the source-drain current by one order of magnitude.[6] Conventional silicon FETs produce S = 60−70 mV/dec,[6] and performance of this caliber has been achieved for CdSe devices in two previous studies—one involving pc-CdSe thin film FETs prepared from CdSe nanocrystals[21] and a second for cadmium-doped NWFETs.[27] S has not been measured and reported for NWFETs prepared from undoped CdSe nanowires, to our knowledge (Table 1). Conventional thin film FETs (not prepared from CdSe nanocrystals) display much higher S values[18−20] ranging from 500 mV/dec[19] to 10 V/dec.[18] For the pc-CdSe NWFETs prepared in this study, S was in the range from 2.3 to 7.1 V/dec. Lower S values were associated with NWFETs prepared from $CdCl_2$-untreated nanowires (Table 1). These are the first and only S values that have been reported for NWFETs prepared from undoped CdSe nanowires.

Device metrics for these NWFETs are strongly influenced by the channel length, L, for both $CdCl_2$-untreated and treated NWFETs (Table 2, Figure 4). As compared with NWFETs having L = 5 μm, NWFETs with L = 10 μm and 25 μm show higher V_{th} (Figure 4b) and S, while the g_m and I_{on}/I_{off} are both substantially reduced (Figure 4a,b). Electron mobilities, μ_{eff}, were also reduced with increasing L, decreasing from 2 (±0.5) × 10^{-3} $cm^2/(V\ s)$ at L = 5 μm to 3 (±2) × 10^{-4} $cm^2/(V\ s)$ for L = 25 μm for $CdCl_2$-treated NWFETs, for example (Figure 4d, green trace).

One reason for the depression in μ_{eff} with increasing L is discontinuities in these nanowires, as shown schematically in Figure 4e−g (top). SEM images (Figure 4e,f, bottom) reveal the presence of discontinuities (circles) in some of the nanowires present in the longer L = 10 and 25 μm channels. Although Figure 4e,f shows data for $CdCl_2$-treated nanowires, these breaks were also observed in untreated pc-CdSe NWFETs, and a similar depression in μ_{eff} was observed in this case (Figure 4c). The majority of these breaks is formed because of stresses applied to the nanowires during the processing steps that succeed annealing, especially the photolithographic patterning of the gold contacts. A similar decrease in μ_{eff} with channel length was also observed by Unalan et al.[64,65] for ZnO NWFETs. We used SEM to determine the number of broken nanowires in our FETs. When the electrically discontinuous nanowires are removed from the total N in eq 3, μ_{eff} increases by a factor of ∼3 for the 10 and 25 μm channels, but the corrected μ_{eff} values (Figures 4c,d, red trace) remain below the values measured for L = 5 μm NWFETs. These data also show that the depression in μ_{eff} is not confined to $CdCl_2$-treated nanowires; a similar effect is seen for nontreated nanowires (Figure 4c). Our hypothesis is that the depression of μ_{eff} for longer channels is caused by the presence of constrictions in the nanowires that are formed during the thermal annealing process. If this is correct, then a remedy might involve the encapsulation of the as-deposited CdSe nanowires in an insulating shell of SiO_2 or another dielectric using atomic layer deposition prior to annealing, to suppress these morphology changes thereby increasing μ_{eff} for these long channel NWFETs.

CONCLUSION

In this paper, we have realized transistors based upon arrays of polycrystalline CdSe nanowires. Uniquely, the LPNE method used to prepare these nanowire arrays permits the patterning of nanowires using photolithography across wafer-scale regions. Two post-processing treatments for these nanowires were compared—the first consisting of thermal annealing only and the second involving exposure to methanolic $CdCl_2$, a grain growth promoter, followed by thermal annealing. The influence of the $CdCl_2$ treatment was significant, increasing the mean grain diameter in pc-CdSe nanowires by a factor of eight from 10 to 80 nm. For both $CdCl_2$-treated and untreated nanowires, the application of a positive gate voltage strongly enhanced conduction; however, NWFETs prepared from $CdCl_2$-treated nanowires showed improved performance highlighted by a reduction in the threshold voltage (∼70%) and the subthreshold slope (∼35%), while the I_{on}/I_{off} ratio was increased by a factor of 3−4. The resulting performance metrics for $CdCl_2$-treated NWFETs are comparable or superior to those of polycrystalline CdSe film-based FETs, but lower μ_{eff} values were obtained for our nanowire devices. A pronounced channel length effect on μ_{eff} suggests that defects in these nanowires such as constrictions may contribute to the depressed electron mobilities. This study demonstrates that highly miniaturized transistors based upon lithographically patterned, electrodeposited polycrystalline nanowires can be prepared.

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Notes

The authors declare no competing financial interest.

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